Question 1

T/F RAID 5 can recover from a two-disk failure.

Question 2

T/F Data dependencies can always be avoided by a bypass logic.

Question 3

T/F ADD instruction requires data memory access.

Question 4

Assume that individual stages of a datapathhave the following latencies:

IF ID EX MEM WB

250ps 200ps 150ps 250ps 200ps

The clock cycle time of pipelined processor is [250];

The clock cycle time of non-pipelined processor is [1050].

Question 5

next PC = PC + \_\_\_ (2/4/16/8)

Question 6

T/F If there are 5 stages in a pipeline, then 5 is the maximum possible speedup.

Question 7

T/F RAW hazard is a control hazard.

Question 8

T/F Magnetic disks are volatile storage devices.

Question 9

Which of the following is correct for a load instruction?

None of the others.

MemtoReg should be set to cause the correct register destination to be sent to the register file.

MemtoReg should be set to cause the data from memory to be sent to the register file.

We do not care about the setting of MemtoReg for loads.

Question 10

T/F As compared to a single-cycled datapath, a pipelined datapath has lower latency and higher throughput.